IN THE SPECIFICATION

Please allow the following amendments to the specification. None of the amendments add new subject matter. They simply correct typographical errors made to the original specification.

Please replace the third paragraph on Page 7, with the following amended paragraph:

Link redundancy is a technique for protecting against the failure of a network line. A networking line may fail for any of a number of reasons (e.g., the line itself may be opened, the aforementioned physical layer devices may ~~mail~~ fail, etc.). As such, networking service providers and networking system providers are interested in technology that allows for such failures without disrupting the operation of a network.

Please replace the second paragraph on Page 12, with the following amended paragraph:

The output of framer logic units 300a and 300c correspond to the inbound signals 304a, 304c from framers 301a and 301c, respectively. That is, the 2:1 multiplexers $308a_1$ through $308a_{xn}$ of framer logic unit 300a are configured to select the framer 301a inbound signals 304a rather than the output signals from the first multiplexer 310a. Similarly, the 2:1 multiplexers $308c_1$ through $308c_{xn}$ of framer logic unit 300c are configured to select the framer 301c inbound signals 304c rather than the output signals from the first multiplexer 310c.

Please replace the third paragraph on Page 12, with the following amended paragraph:

The first (xn):n multiplexer 310b within framer logic unit 300b is configured to select the output signals from framer logic unit 300a. Also, the first (xn):n multiplexer 310d within framer logic unit 300d is configured to select the output signals from framer logic unit ~~300b~~ 300c. As such, first multiplexer 310b effectively presents framer 301a inbound signals 304a to the 2:1 multiplexers 350 within framer logic unit 300b; and first multiplexer 310d effectively presents framer 301c inbound signals 304c to the 2:1 multiplexers 360 within framer logic unit 300d.

A2

Please replace the first paragraph on Page 13, with the following amended paragraph:

The 2:1 multiplexers 350, 360 of frame logic units 300b, ~~300c~~ 300d also receive the inbound signals 304b, 304d from their respective framers 301b, 301d. As such, the 2:1 multiplexers 350 receive the inbound signals 304b from framer 301b at one channel input as well as receive the inbound signals 304a from framer 301a at the other channel input. Similarly, the 2:1 multiplexers 360 receive the inbound signals 304d from framer 301d at one channel input as well as receive the inbound signals 304c from framer 301c at the other channel input.

A3

Please replace the first full paragraph on Page 15 with the following amended paragraph:

Figure 5 shows another framer logic unit embodiment 500 that may be viewed as the framer logic unit 200 of Figure 2 further including a switching or routing extension 501. The inputs 212_1, 212_2, 212_3, . . . , 212_x to the framer logic unit 500 are coupled to a third (xn):n multiplexer 503 that may select any inbound signal for switching or routing. Routing or switching engine 501 provides packet based (e.g., Internet Protocol (IP) based) switching (e.g., label switching) or routing. The routing or switching engine ~~502~~ 501 may be a logic circuit; or a processor that executes software consistent with the routing or switching protocol(s) to be employed; or a combination of logic and processor.

Please replace the second full paragraph on Page 15 with the following amended paragraph:

The routing or switching engine ~~502~~ 501 assembles packets from the signals 505_1, 505_2, 505_3, . . . , 505_n selected by a third (xn):n multiplexer 503. Based on the destination of a packet (e.g., as indicated in the packet's header), the routing or switching engine ~~502~~ 501 determines an appropriate outbound signal 506_1, 506_2, 506_3, . . . , 506_n that the packet should be forwarded to. The packet is then disassembled and sent over the appropriate outbound signal. Note that a second framer logic unit output 502 may be viewed as a bus having each of the switching or routing engine output signals 506_1, 506_2, 506_3, . . . , 506_n.